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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/760,640
Filing Date: January 20, 2004
Appellant(s): DOREN ET AL.

Gary J Pitzer
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 6, 2008 appealing from the Office action mailed April 18, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

10/760,599; 10/760,652; 10/760,659; 10/760,813; and 10/761,073.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6138218 Arimilli 10-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 11-13, 15-21, and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Glasco (2005/0251626).

As per claim 1, Glasco discloses a system comprising: a first node having an associated cache including data having an associated first cache state, the first cache state being capable of identifying the first node as being an ordering point for serializing requests from other nodes for the data [par. 45, ll 1-3; par. 87, ll 11-16; pars. 120-123].

As per claim 2, Glasco discloses the first cache state enables the first node to provide a data response to a request for the data from a second node for the data without updating a system memory, the data response comprising a copy of the data

requested from the second node [pars. 131, 0116, 0118, 0120].

As per claim 3, Glasco discloses the first cache state enables the first node to provide an ownership data response to a request for the data from a second node, the ownership data response transferring the ordering point from the first node to the second node [pars. 89-90].

As per claim 4, Glasco discloses the first node provides the ownership data response without updating a system memory [par. 131].

As per claim 5, Glasco discloses the first node defines a first processor and the second node defines a second processor [Fig. 2], each of the first processor and the second processor having an associated cache [par. 3], ll 6-9], the associated caches of the first and second processors each comprising a plurality of cache lines [Abstract], each cache line having a respective tag address that identifies associated data and each cache line having state information that indicates a state of the associated data for the respective cache line [par. 59], the first and second processors being capable of communicating with each other and with other nodes of the system through an interconnect [Fig. 1B, Switch 131; par. 0051].

As per claim 6, Glasco discloses a first cache controller associated with the first processor and a second cache controller associated with the second processor [Fig. 2,

Controller 230], the first cache controller being operative to manage data requests and responses for the associated cache of the first processor [Abstract], the first cache controller effecting state transitions associated with the data in the associated cache of the first processor based on the data requests and responses for the associated cache of the first processor [par. 10], the second cache controller being operative to manage data requests and responses for the associated cache of the second processor [par. 12], the second cache controller effecting state transitions associated with the data in the associated cache of the second processor based on the data requests and responses for the associated cache of the second processor [par. 15].

As per claim 11, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 12, the rationale in the rejection of claim 2 is herein incorporated.

As per claim 13, the rationale in the rejection of claim 3 is herein incorporated.

As per claim 15, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 16, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 17, the rationale in the rejection of claim 2 is herein incorporated.

As per claim 18, the rationale in the rejection of claim 3 is herein incorporated.

As per claim 19, the rationale in the rejection of claims 1 and 3 is herein incorporated.

As per claim 20, the rationale in the rejection of claim 2 is herein incorporated.

As per claim 21, the rationale in the rejection of claim 3 is herein incorporated.

As per claim 24, the rationale in the rejection of claim 1 is herein incorporated.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 8, 9, and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glasco (2005/0251626) in view of Arimilli (6,138,218).

As per claim 7, Glasco discloses the claimed invention as discussed above.

However, Glasco does not explicitly teach a third node retries the source broadcast request employing a forward progress protocol as required.

Arimilli discloses a third node retries the source broadcast request employing a forward progress protocol [col. 1, ll 6-12; col. 1, lines 13-14; col. 1, lines 33-41; col. 5, lines 19-54] in order to allow other traffic to proceed and alleviate the prospect of a livelock (col. 1, ll 13-14).

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by Applicant, to modify the system of Glasco to include a third node retrying the source broadcast request employing a forward progress protocol since this would have allowed other traffic to proceed and alleviated the prospect of a livelock (col. 1, ll 13-14) as taught by Arimilli.

As per claim 8, Arimilli discloses the forward progress protocol comprises a null-directory protocol [col. 1, ll 6-12; col. 1, lines 13-14; col. 1, lines 33-41; col. 5, lines 19-54;].

As per claim 9, Glasco discloses the source broadcast protocol comprises an incomplete protocol [par. 4, ll 9-11].

As per claims 22 and 23, the rationale in the rejection of claim 7 is herein incorporated.

Allowable Subject Matter

Claims 10 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(10) Response to Argument

Appellant's argument on page 12 that "since Glasco teaches that the home memory controller is the serialization point for transactions to memory lines in the coherence directory regardless of the cache state for such memory lines, Glasco does not anticipate claim 1" is clearly erroneous.

Examiner would like to first make it clear that though the prior art must disclose the claimed invention in as complete detail as is contained in the claims, this is not however an ipsissimis verbis test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Though the prior art may use terms similar to that of applicants' claimed invention, it also suffices that the prior art discloses the claimed subject matter at least in the manner recited in applicants' specification.

Claim 1 simply recites:

"A system comprising: a first node having an associated cache including data having an associated first cache state, the first cache state being capable of identifying the first node as being an ordering point for serializing requests from other nodes for the data."

As described on page 8, paragraph [0033] of the specification, "the state of a cache line can be utilized to define a cache ordering point in a system. In particular, for a protocol implementing the states set forth in Table 1 (I, S, E, F, D, M, O), a cache line having one of the states M, O, E, F, or D can serve as an ordering point for the data contained in that cache line. In particular, a cache line having any one of the states M, O, and D must implement a write-back to memory upon displacement of the associated data. As a result of implementing the write-back, a cache ordering point for a given cache line will migrate from the cache of an associated processor to memory so that the memory contains a coherent copy of the data".

As described on page 12, paragraph [0042] of the specification, "a target node can provide an ownership data response that includes D-DATA, for example, when the processor has an ownership state (e.g., M, O, E, F, or D) associated with the cached data in the SSP protocol. It is the state of the cached data that defines the node (processor) as a cache ordering point for the data. When a processor responds with D-DATA, the ordering point is transferred to the requesting processor. S-DATA is a shared data response that indicates data is being returned from a cache ordering point, although the ordering point itself is not being transferred to the requester. An S-DATA response also indicates that a copy of the data may be in one or more other caches. An M-DATA response can be provided by memory (e.g., a home node) by returning the present value for the data stored in memory."

Glasco unequivocally discloses as detailed on page 3 of the Office action mailed on October 6, 2006, and at least in paragraphs [0087, 0091] and paragraphs [0116, 0120-0123], "a system having a cache coherency directory where cache lines have states including modified (M), owned (O), shared (S), dirty (D), and invalid (I). If the directory entry indicates that the line is in the "dirty" state, the modified memory line to memory must first be written back to memory; the eviction of a cache coherency directory entry corresponding to a "dirty" line in a remote cache requires that the remote cache writes the line back to memory".

In Fig. 3 Glasco depicts a cache coherence controller 230 of a node including a protocol engine that allows the cache coherence controller to track transactions including tags and state information [pars. 0058-0059], wherein Fig. 5A shows that cache coherence controller acting as an aggregate cache, wherein upon a data access request, that cache controller accepts a probe from a local memory and forward it to a non-local portion wherein the probe can carry information that allows the caches to properly transition the cache state for a specified line [Fig. 5A, par. 0065; Fig. 17, pars 0149-0150]; and a cache line having either a modified (M), Owned (O), or dirty (D) state and a write-back to memory upon displacement (i.e., line is dirty or evicted) and consequently when the processor responds with a dirty data, the ordering point is transferred to the requesting processor [pars. 0120-0123]. The state of the data in that node (i.e., M, O, D) is what defines that node as the ordering point.

Thus, it is manifest that Glasco discloses, as claimed by applicants, "a cache state being capable of identifying the first node as an ordering point for serializing requests from other node for the data" when a cache line having either a modified (M), Owned (O), or dirty (D) state and a write-back to memory upon displacement (i.e., line is dirty or evicted) and consequently when the processor responds with a dirty data, the ordering point is transferred to the requesting processor.

Glasco discloses a system comprising: a first node having an associated cache including data having an associated first cache state, the first cache state being capable of identifying the first node as being an ordering point for serializing requests from other nodes for the data [*a system in which cache coherency can be maintained by sending all data access requests through a serialization (i.e., ordering) point*; par. 0045; *a cluster (node) containing a serialization point is referred to as a home cluster (node)*; par. 0064; *coherence directory including state information, the memory line states are modified, owned, shared, and invalid*; pars. 0087-0089; *eviction of a cache entry corresponding to a dirty line in a remote cache requires that the remote cache write the line back to memory and invalidate its copy*; pars. 0120-0123].

Furthermore, appellant argues on page 15 that "it is data in the associated cache of the first node that identifies the first node as the ordering point, whereas in Glasco, it is the entries in a coherence directory of a memory controller for multiple processors that indicate the state of the line".

However, as evident from the claim language itself "...the first cache state {is what is} being capable of identifying the first node as being an ordering point

for serializing requests from other nodes for the data". Thus, there is "an associated cache which includes data" and there is "cache state associated with that data". In claim 1, it is "the state of the cache" that identifies the node as the ordering point "not the data in the associated cache" as assumed by appellant.

Furthermore, in Fig. 5A Glasco shows that cache coherence controller acting as a cache, wherein upon a data access request, that cache controller accepts a probe from a local memory and forward it to a non-local portion wherein the probe can carry information that allows the caches to properly transition the cache state for a specified line [Fig. 5A, par. 0065; Fig. 17, pars 0149-0150] and in paragraphs [0120-0123] shows data associated with cache in a first node, depending upon which state the data is in, identifying that node as the ordering point [0116, 0118, 0119-0123].

Appellant's argument on page 15, paragraph 2, that there is nothing in Glasco to suggest that "an ordering point is transferred when a write back to memory occurs" is clearly in error.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "an ordering point is transferred when a write back to memory occurs") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not

read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Glasco teaches "in a cluster system, requests are generated to specific processors to invalidate cache entries and to write cache entries back to memory; if the directory entry indicates that the line is in the dirty state in any of the remote caches, the modified memory line to memory must first be written back to memory before the line is invalidated in each of the remote caches; paragraphs [0116, 0118, 0120]".

Appellant's arguments on page 16, paragraph 1, with respect to claim 2, that Glasco does not involve any "data response that includes a copy of the requested data" and "since the process being described is an eviction of clean (as opposed to dirty) memory line, no data response is provided and no data is written back to memory as part of the eviction process" are clearly erroneous.

Glasco teaches "in a cluster system, requests are generated to specific processors to invalidate cache entries and to write cache entries back to memory; if the directory entry indicates that the line is in the dirty state in any of the remote caches, the modified memory line to memory must first be written back to memory before the line is invalidated in each of the remote caches; paragraphs [0116, 0118, 0120]".

Appellant's argument on page 19, paragraph 3, with respect to claim 1, that "the rejection of claim 5 is deficient with regard to identifying structure that enables communication between processors" is clearly in error.

> Glasco shows in Fig. 1B and paragraph [0051], processing clusters 121-127 being capable of communicating with each other or any other clusters through switch 131; each processing cluster 121, 123, 125, and 127 can be coupled to a switch 131.

Appellant's arguments on page 21, with respect to claim 7 that Arimilli does not provide for "each processor to reissue a request for specific data by employing a forward progress protocol if the request fails in the source broadcast protocol" are clearly in error.

> The reissuing of the request employing a forward progress protocol is done using "a hybrid cache coherency protocol, such as a broadcast source snoop protocol implemented in conjunction with a forward progress (e.g., directory-based or null-directory) protocol (See applicant's disclosure at paragraph 0029)". In the same manner, Arimilli discloses "snoop operations which are retried and making forward progress on retried snoop operations; col. 1, lines 13-14; coherency of the storage hierarchy is maintained through the use of a selected memory coherency protocol such as the MESI protocol; the

coherency state is indicated by bits in the cache directory; col. 1, lines 33-41; and in Fig. 2A-2C, a mechanism for making forward progress on retried snoop; a first device initiates a read or rwitm operation, upon detected the read or rwitm operation, I2 cache asserts an intervention response, however, intervention response is impeded by a second device, asserting a retry; I2 cache 114 initiates an action altering the coherency state associated with requested cache item or initiate a push operation to write (modified) requested cache item; the push operation may be snooped off the system bus by other devices; col. 5, lines 19-54.

Appellant's assumption with respect to claim 8 that Arimilli fails to teach or suggest that "the mechanism used to achieve forward progress corresponds to null directory protocol" is clearly erroneous.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "the mechanism used to achieve forward progress corresponds to null directory protocol") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Arimilli discloses "snoop operations which are retried and making forward progress on retried snoop operations; col. 1, lines 13-14; coherency of the storage hierarchy is maintained through the use of a selected memory coherency protocol such as the MESI protocol; the coherency state is indicated by bits in the cache directory; col. 1, lines 33-41; and in Fig. 2A-2C, a mechanism for making forward progress on retried snoop; a first device initiates a read or rwitm operation, upon detected the read or rwitm operation, I2 cache asserts an intervention response, however, intervention response is impeded by a second device, asserting a retry; I2 cache 114 initiates an action altering the coherency state associated with requested cache item or initiate a push operation to write (modified) requested cache item; the push operation may be snooped off the system bus by other devices; col. 5, lines 19-54.

Finally, it is worth mentioning that several limitations are statements of intended use of the claimed invention. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

For instance: Independent claim 1 recites, "A system comprising: a first node having an associated cache including data having an associated first cache

state, the first cache state being capable of identifying the first node as being an ordering point for serializing requests from other nodes for data". Independent claim 24 recites "A coherency protocol operative to assign a cache state to a cache line of one node of a plurality of nodes of a system, the cache state defining the one node as an ordering point in the system for data in the cache line of the one node".

See, e.g., In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963) (The claims were directed to a core member for hair curlers and a process of making a core member for hair curlers. Court held that the intended use of hair curling was of no significance to the structure and process of making.); In re Sinex, 309 F.2d 488, 492, 135 USPQ 302, 305 (CCPA 1962) (statement of intended use in an apparatus claim did not distinguish over the prior art apparatus). A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If a prior art structure is capable of performing the intended use as recited in the preamble, then it meets the claim. See, e.g., In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997). See also MPEP § 2112 - § 2112.02. MPEP 2114.

Furthermore, while features of a system may be recited either structurally or functionally, claims directed to a system must be distinguished from the prior art in terms of structure rather than function. *In re Schreiber*, 128 F.3d 1473,

1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< *In re Danly,* 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "System claims cover what a device *is*, not what a device *does*." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In view of the foregoing, it is manifest that the claimed invention is not patentably distinct over the combinations of Glasco (2005/0251626) and Arimilli (6,138,218) when interpreted in light of the specification, given the claims their broadest reasonable interpretation in view of applicant's disclosure, and taken into account legal standards for determining obviousness under 35 U.S.C. 103 in view of the Supreme Court decision In re *KSR International Co. v. Teleflex Inc.,* 550 U.S. at_,82 USPQ2d at 1396 (2007).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Mardochee Chery MC
Examiner

Conferees:

/Hyung Sough/ HS
Supervisory Patent Examiner
07/29/08

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